SPECIFICATION AMENDMENTS

The paragraph beginning at line 19 on page 3 is revised as follows:

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for fabricating a double gate MOSFET. The method includes providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer, a first spacer or separation layer disposed on the first insulation layer, and a semiconductor layer disposed on the first spacer layer. The semiconductor layer is patterned resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET. A second spacer or separation layer is deposited on the semiconductor layer structure and the first spacer layer. The first and second spacer layers are patterned such that the semiconductor layer structure remains substantially completely embedded in the first and second spacer layers. A second insulation layer is deposited on a structure formed of the first and second spacer layers. Two depressions disposed along one direction are vertically etched, the two depressions are dimensioned such that the semiconductor layer structure is situated completely between them. During the etching of the two

depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure are etched through completely in each case. The depressions are filled with an electrically conductive material. A contact hole is formed in the second insulation layer. The first and second spacer layers are selectively removed through the contact hole made in the second insulation layer. Third insulation layers are applied on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure. A further electrically conductive material is introduced into the region of the removed spacer layers.